

Applicant's semiconductor device includes a guard ring pattern to prevent moisture from intruding into a semiconductor integrated circuit. Base claim 1 specifies that the semiconductor device has a guard ring pattern that includes:

[a] conductive wall changing a direction thereof repeatedly and alternately in one of a triangular wave pattern and a rectangular wave pattern.

Claims 2-4 and 7 depend from claim 1, so they include this feature by virtue of their dependency. The applied prior art does not suggest such a semiconductor device.

Accordingly to the Office Action, the rejection relies on the *APA* guard ring structure 12 to teach a guard ring pattern, but it is acknowledged that this structure does not change direction repeatedly and alternately as claimed. Therefore, to justify the obviousness rejection relying on *APA* as the primary reference, a suggestion must be provided to modify the guard ring structure 12 to change direction repeatedly and alternately. Applicant respectfully submits that such a suggestion is not provided in the Office Action.

The rejection relies on *Cook et al.* to suggest modifying the *APA* guard ring structure 12 to change direction repeatedly and alternately as claimed. Applicant acknowledges the *Cook et al.* disclosure of conductor patterns 60 and 70 in Figs. 5a and 8a, respectively. Applicant also acknowledges that *Cook et al.* explains in col. 1, lines 13-40, that dicing semiconductor wafers was known to cause the problem of cracks propagating across chips into the active device area (note Fig. 2), which leads to chip failure. Applicant further acknowledges that *Cook et al.* professes to solve the problem of crack propagation in col. 4, lines 4-19, by forming conductor 60 into a serpentine ring.

As noted previously, the purpose of the *Cook et al.* guard ring, to prevent crack propagation during wafer dicing, differs from applicant's purpose to prevent moisture intrusion into a semiconductor integrated circuit. The *Cook et al.* configuration would not be so effective

in preventing moisture intrusion because of the following:

As shown in Figs. 4b, 5c, 6b, and 7c, the *Cook et al.* embodiments have air-filled trenches in the top passivation film. Consequently, the top of the outer ring patterns are exposed to atmosphere. Therefore, although according to the *Cook et al.* its disclosed guard ring pattern effectively interrupts propagation of delamination cracks in thin film layers (Abstract), the guard ring pattern cannot block moisture penetration. Instead, moisture would be able to penetrate into the region where the passivation film is disconnected.

Such is not a problem in applicant's semiconductor device. Base claim 1 even specifies that:

said conductive pattern and said second insulation film located at a top part of said multilayer interconnection structure being *covered continuously with an insulation film* [emphasis added].

That is, applicant's semiconductor device has a protection against moisture penetration that is not disclosed by *Cook et al.* The Office Action provides no reason why one skilled in the art would supposedly want to adopt only part of the *Cook et al.* teachings needed to yield the *Cook et al.* benefit.

Accordingly, because *Cook et al.* cannot be properly relied upon to suggest modifying the *APA* device to have the claimed structure, the obviousness rejection should be withdrawn.

In view of the remarks above, applicant now submits that the application is in condition for allowance. Accordingly, a Notice of Allowability is hereby requested. If for any reason it is felt that this application is not now in condition for allowance, the Examiner is invited to contact applicant's undersigned attorney at the telephone number indicated below to arrange for disposition of this case.

In the event that this paper is not timely filed, applicant petitions for an appropriate extension of time. The fees for such an extension, or any other fees which may be due, may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP



Joseph L. Felber  
Attorney for Applicant  
Reg. No. 48,109

Atty. Docket No. **000294**  
1250 Connecticut Avenue, N.W., Suite 700  
Washington, DC 20036  
Tel: (202) 822-1100  
Fax: (202) 822-1111

Enclosure: Petition for extension of time

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